IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: McArthur et al

Patent No.: 7,099,011
Issued: August 29, 2006

Serial No.: ~~10/727,081~~ 10/724,018
Filed: December 2, 2003

Conf. No.: 4422
Customer No.: 33123

For: METHOD AND APPARATUS FOR SELF-REFERENCED PROJECTION LENS DISTORTION MAPPING

Art Unit: 2877

Examiner: Gordon j. Stock, Jr.

CERTIFICATE OF MAILING

I hereby certify that this correspondence and the attached papers are being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated below and addressed to:

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

9-7-06
Date

Jennifer Ward
Signature

REQUEST FOR CERTIFICATE OF CORRECTION PURSUANT TO 37 C.F.R. § 1.322

Attn: Certificate Of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.322, the patentee respectfully requests that a Certificate of Correction be issued for the above-referenced patent.

REMARKS

A Certificate of Correction (Form PTO-1050), in duplicate, is included with this Request.

This Certificate of Correction seeks to correct obvious typographical and grammatical errors in the specification of the issued patent. During prosecution, a "Preliminary Amendment" was filed on March 18, 2004 (copy enclosed). The return postcard was received from OIPE indicating that the Preliminary Amendment was received on March 22, 2005. The amendments to specification from the Preliminary Amendment are not reflected in the printed patent.

No new matter has been added. Approval of the proposed correction and issuance of the Certificate of Correction are respectfully requested.

The Commissioner is authorized to charge the filing fee of **$100.00** for the Certificate of Correction, and to charge any additional fees that may be required, or to credit any refund, to Deposit Account No. **50-1213**, referencing Attorney's Docket No. **38203-6080C**.

Respectfully submitted,
Heller Ehrman LLP

Steven A. Moore
Registration No. 55,462

Attorney Docket No. 38203-6080C
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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 3, line 32 to column 4, line 4, please amend as follows:

--Semiconductor manufacturing facilities generally use some version of the following complex overlay procedure to help determine the magnitude of lens distortion independent of other sources of systematic overlay error. The technique has been simplified for illustration. *See* Analysis of image field placement deviations of a 5x microlithographic reduction lens, D. MacMillen, et al., SPIE Vol. 334, 78:89, 1982. FIGS. 2 and 3 show typical sets of overlay targets 300, including – one large or outer box 302 and one small or inner target box 304. FIG. 1 shows a typical portion of a distortion test reticle 102 used in the prior art. It should be noted that the chrome target patterns on most reticles are 4 or 5 times larger as compared with the patterns they produce at the image ~~plane,~~ plane; this simply means modern steppers are reduction systems. Further, for purposes of discussion, it is assumed that the reticle pattern is geometrically perfect, (in practice, the absolute positions of features on the reticle can be measured and the resulting errors subtracted off). First, a wafer covered with photoresist is loaded onto the wafer stage and globally aligned. Next, the full-field image of the reticle, 102 in FIG. 1 is exposed onto the resist-coated wafer 2102 in FIG. 21. For purposes of illustration, we assume that the distortion test reticle consists of a 5 x 5 array of outer boxes evenly spaced a distance M*P, across the reticle surface see FIG. 1. It is typically assumed that the center of the optical system is virtually aberration free. *See* Analysis of image field placement deviations of a 5x microlithographic reduction lens, *supra*. With this assumption, the reticle, 102 in FIG. 1 is now partially covered using the reticle blades, 1704 in FIG. 17, in such a way that only a single target at the center of the reticle field, box 104, in FIG. 1, is available for exposure. Next, the wafer stage is moved in such a way as to align the center of the reticle pattern directly over the upper left hand corner of the printed 5 x 5 outer box array, wafer position 2100, FIG. 21. The stepper then exposes the image of the small target box onto the resist-coated wafer. If the stepper stage and optical system were truly perfect then the image of the small target box would fit perfectly inside the image of the larger target box, as illustrated in FIGS. 4, and 21, from the previous exposure.--

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Column 5, lines 1-25, please amend as follows:

--(artifact) with a rectangular array of measurable targets on a stage and measuring the absolute positions of the targets using a tool stage and the tool's image acquisition or alignment system. This measurement process is repeated by reinserting the artifact on the stage but shifted by one target spacing in the X-direction, then repeated again with the artifact inserted on the stage shifted by one target spacing in the Y-direction. Finally, the artifact is inserted at 90-degrees relative to its initial orientation and the target positions measured. The resulting tool measurements are a set of (x, y) absolute positions in the tool's nominal coordinate system. Then, the absolute positions of both targets on the artifact and a mixture of the repeatable and non-repeatable parts of the stage x, y grid error are then determined to within a global translation (Txg, Tyg), rotation (qg) and overall scale ((sxg+syg)/2) factor. This technique is not directly applicable to the present situation since it requires that the measurements be performed on the same machine that is being assessed by this technique. Furthermore, this prior art technique requires measurements made on a tool in absolute coordinates; the metrology tool measures the absolute position of the printed targets relative to ~~it's~~ its own nominal center; so absolute measurements are required over the entire imaging field (typical size >~ 100 mm^2). --

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INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 7, lines 41-54, please amend as follows:

--Overlay error is referred to as overlay registration ~~include~~ including, registration error and pattern placement ~~error,~~ error; for our work here, we will simply use the term overlay error or error. For classification purposes, overlay error is typically divided into the following two categories: grid or inter-field and intra-field error. Intra-field error is the overlay error in placement within a projection field, or simply field, of a lithographic projection system. Inter-field error is the overlay error from field to field on the wafer. The physical sources of these errors are generally distinct; inter-field error is due to imaging objective aberrations or possibly scanning dynamics while intra-field errors are due to the wafer alignment system and the wafer stage. The focus of this invention is determination of intra-field error.--

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IN THE SPECIFICATION

Column 8, lines 1-42, please amend as follows:

--Lithography systems, T. Hasan, et al., IEEE Transactions on Electron Devices, Vol. ED-27, No. 12, 2304:2312, December, 1980; Capacitor Circuit Structure For Determining Overlay Error, K. Tzeng, et al., US Patent 6,143,621, 2000; Overlay Alignment Measurement of Wafers, N. Bareket, US Patent 6,079,256, 2000. The present invention applies to photolithographic steppers, scanners, e-beam systems, EUV and x-ray imaging systems. *See* Mix-And-Match: A necessary Choice, *supra*; Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron, J. Bjorkholm, et al., Journal Vacuum Science and Technology,B 8(6), 1509:1513, Nov/Dec 1990; Development of XUV projection lithography at 60-80 nm, B. Newnam, et al., SPIE vol. 1671, 419:436, 1992; Optical Lithography – Thirty years and three orders of magnitude, J. Bruning, SPIE Vol. 3051, 14:27, 1997. FIG. 28 shows a typical vector plot of overlay error measured with a commercial overlay tool using box-in-box structures. In some cases the overlay error can be measured using special in-situ exposure tool metrology. *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, M. Van den Brink, et al., SPIE VOL. 1087, 218:232, 1989. Vector displacement plots like these illustrated in FIG. 28 give a visual description of the direction, magnitude, and location of overlay error, and are mathematically separated into components using a variety of regression routines; FIGS. 28- 30 are a schematic of this while ~~*See*~~ Analysis of overlay distortion patterns, J. Armitage, J. Kirk, SPIE Vol. 921, 207:221, 1988 contains numerous examples. Many commercial software packages exist (Monolith, *See* A Computer Aided Engineering Workstation for registration control, *supra*., Klass II; *See* Lens Matching and Distortion testing in a multi-~~stepper~~ stepper, sub-micron environment, A.Yost, et al., SPIE Vol. 1087, 233:244, 1989) that model and statistically determine the relative magnitude of the systematic and random inter-field and intra-field error components for the purpose of process control and exposure tool set-up. Once the inter-field and intra-field overlay data is analyzed the results are used to adjust the calibration constants and absolute position of the reticle stage, wafer handling stage and projection lens system to improve pattern alignment.--

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Column 9, lines 56-57, please amend as follows:

--Then in block 3416 we reconstruct the overlay measurements that are used to produce the lens distortion map.--

Column 12, lines 16-28, please amend as follows:

--In another embodiment, if it is believed or there is evidence that the wafer stage and reticle alignment system are extremely accurate and repeatable (for example if the accuracy and repeatability <~ overlay metrology tool accuracy and repeatability), then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx4,Ty4,q4) can be set to zero in equations 5-8. Not solving for the T's and q's allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution that includes field rotation, orthogonality, and x and y scale is obtained if the constraints of equation 9 and equation 10 through equations 14 and 15 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=qo=sx=sy=0 in equations 20 and 21.

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Column 16, lines 63-67, please amend as follows:

--With regard to error multipliers, the effect of including the R-shears in these calculations is to further reduce the error multipliers from the X, Y shear case since including more measurements increases the averaging of overlay metrology tool noise and thereby decreases ~~it's~~ its influence.--

Column 17, lines 7-20, please amend as follows:

--In another embodiment, if ~~its~~ it is believed, or there is evidence, that the wafer stage and reticle alignment system are extremely accurate and repeatable, for example if the accuracy and repeatability <~ overlay metrology tool accuracy / repeatability, then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx6,Ty6,q6) can be set to zero in equations 27-32. Not solving for the T's and q's allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution is obtained that includes field rotation and overall scale if the constraints of equation 33 and equation 34 through equations 37 and 38 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=s=0 in equations 41 and 42.--

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IN THE SPECIFICATION

Column 18, lines 28-53, please amend as follows:

--A variation of the first two embodiments that allows the user to extract the repeatable part of the intra-field distortion with a minimum number of exposed fields and overlay metrology is described. Below, Eo is the E-zero or minimum exposure dose required for a large, i.e. 200 micron at wafer, open area pattern on the reticle to become fully developed, or cleared in the case of positive resist. FIG. 34A illustrates a process flow diagram where in blocks 3442, 3444 and 3446, the overlay target reticle and resist coated wafer are loaded into the projection imaging tool, or machine, as described above. Next in blocks 3448 and 3450, instead of exposing each field with a single scanning or exposing action, the machine is programmed to expose each field at a multiplicity of lower doses. So if a*Eo (a > 1) is the required dose at the wafer to completely expose a single field with a single exposing action, we expose the field N times at a dose of a*Eo/N, where N is some predetermined number, typically 20. Within these N exposures the wafer stage is not moved to another field position, a single field is exposed N times. In the preferred embodiment, this process is repeated 3 more times for the other fields. The result of this procedure is to average out the scanning non-repeatability by an amount proportional to N (parameterized as b*M). The exact configuration of the resist (novolac, chemically amplified, resist manufacturer, processing conditions) determines whether b =1 or is < 1.--

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Column 18, lines 58-67, please amend as follows:

--Then in blocks 3452, 3454, and 3456 the wafer is developed and the overlay targets ~~and~~ are measured and a lens distortion map constructed as described above in connection with FIG. 34.

In another variation of the first two embodiments, multiple exposing actions are performed to average out the effect of non-repeatability, but now the overlay reticle, for example the reticle of FIG. 20, has a partially reflecting dielectric coating either on ~~it's~~ its non-chrome or possibly chrome coated (machine optical object plane) surface see FIG. 20C. For --

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IN THE SPECIFICATION

Column 19, lines 40-57, please amend as follows:

--The techniques described above have been mainly described with respect to alignment attributes that are in the form of a box in box or frame in frame pattern as shown in FIG. 14. Other alignment attributes such as gratings can be used. *See* U.S. Pat. No. 6,079,256 - Overlay Alignment Measurement of Wafer, *supra*, and FIG. 1b, wafer alignment marks. *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, *supra*, van der Pauw resistors. *See* Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography systems, *supra*, vernier pairs; *See* Method of Measuring Bias and Edge overlay error for sub 0.5 micron Ground Rules, C. Ausschnitt, et al., U.S. Pat. No. 5,757,507 (1998), capacitor structures. *See* Capacitor Circuit Structor For Determining Overlay Error, *supra* could be used instead. In general, any alignment attribute that can be used by an overlay metrology tool for measuring offsets can be utilized by the techniques described.--

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IN THE SPECIFICATION

Column 25, line 51 to column 26, line 20, please amend as follows:

--The techniques have been mainly described with respect to ~~it's~~ their application on the projection imaging tools such as photolithographic stepper ~~systems~~ systems. *See* Direct-referencing automatic two-points reticle-to-~~wafer~~ wafer alignment using a projection column servo system, *supra*; New 0.54 Aperture I-Line Wafer Stepper With Field by Field Leveling Combined with Global Alignment, M. Van den Brink, B. Katz, S. Wittekoek, SPIE Vol. 1463, 709:724, 1991; Projection optical system for use in precise copy, T. Sato, et al., U.S. Pat. No. 4,861,148, 1989, and photolithographic scanners systems. *See* Micrascan (TM) III performance of a third generation, catadioptric step and scan lithographic tool, D. Cote, et al., SPIE Vol. 3051, 806:816, 1997; ArF Step And Scan Exposure System For 0.15 Micron and 0.13 micron Technology Node, J. Mulkens, et al., SPIE Conference on Optical Microlithography XII, 506:521, March, 1999; 0.7 NA DUV step and Scan system for 150nm Imaging with Improved Overlay, supra ~~*supra*~~]) most commonly used in semiconductor manufacturing today. The techniques can be applied to other projection imaging tools such as contact or proximity printers. *See* Optical Lithography--Thirty years and three orders of magnitude, *supra*, 2-dimensional scanners; *See* Large-area, High-throughout, High-Resolution Projection Imaging System, K. Jain, U.S. Pat. No. 5,285,236, 1994, Optical Lithography--Thirty years and three orders of magnitude, *supra*, office copy machines, and next generation lithography (ngl) systems such as XUV. *See* Development of XUV projection lithography at 60-80 nm, *supra*, SCALPEL, EUV (Extreme Ultra Violet); *See* Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron ef 53, *supra*, IPL (Ion Projection Lithography), and EPL (electron projection lithography). *See* Mix-And-Match: A necessary Choice, *supra*. In addition, the techniques can be applied to a lithographic projection system used in an electron beam imaging system, or a direct write tool, or an x-ray imaging system.--

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,099,011

APPLICATION NO. : ~~10/727,081~~ 10/724,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 7, lines 41-54, please amend as follows:

--Overlay error is referred to as overlay registration ~~include~~ including, registration error and pattern placement ~~error,~~ error; for our work here, we will simply use the term overlay error or error. For classification purposes, overlay error is typically divided into the following two categories: grid or inter-field and intra-field error. Intra-field error is the overlay error in placement within a projection field, or simply field, of a lithographic projection system. Inter-field error is the overlay error from field to field on the wafer. The physical sources of these errors are generally distinct; inter-field error is due to imaging objective aberrations or possibly scanning dynamics while intra-field errors are due to the wafer alignment system and the wafer stage. The focus of this invention is determination of intra-field error.--

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PATENT NO. : 7,099,011

APPLICATION NO. : ~~10/727,081~~ 10/714,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 8, lines 1-42, please amend as follows:

--Lithography systems, T. Hasan, et al., IEEE Transactions on Electron Devices, Vol. ED-27, No. 12, 2304:2312, December, 1980; Capacitor Circuit Structure For Determining Overlay Error, K. Tzeng, et al., US Patent 6,143,621, 2000; Overlay Alignment Measurement of Wafers, N. Bareket, US Patent 6,079,256, 2000. The present invention applies to photolithographic steppers, scanners, e-beam systems, EUV and x-ray imaging systems. *See* Mix-And-Match: A necessary Choice, *supra*; Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron, J. Bjorkholm, et al., Journal Vacuum Science and Technology,B 8(6), 1509:1513, Nov/Dec 1990; Development of XUV projection lithography at 60-80 nm, B. Newnam, et al., SPIE vol. 1671, 419:436, 1992; Optical Lithography – Thirty years and three orders of magnitude, J. Bruning, SPIE Vol. 3051, 14:27, 1997. FIG. 28 shows a typical vector plot of overlay error measured with a commercial overlay tool using box-in-box structures. In some cases the overlay error can be measured using special in-situ exposure tool metrology. *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, M. Van den Brink, et al., SPIE VOL. 1087, 218:232, 1989. Vector displacement plots like these illustrated in FIG. 28 give a visual description of the direction, magnitude, and location of overlay error, and are mathematically separated into components using a variety of regression routines; FIGS. 28- 30 are a schematic of this while *See* Analysis of overlay distortion patterns, J. Armitage, J. Kirk, SPIE Vol. 921, 207:221, 1988 contains numerous examples. Many commercial software packages exist (Monolith, *See* A Computer Aided Engineering Workstation for registration control, *supra*., Klass II; *See* Lens Matching and Distortion testing in a multi-~~stepper~~ stepper, sub-micron environment, A.Yost, et al., SPIE Vol. 1087, 233:244, 1989) that model and statistically determine the relative magnitude of the systematic and random inter-field and intra-field error components for the purpose of process control and exposure tool set-up. Once the inter-field and intra-field overlay data is analyzed the results are used to adjust the calibration constants and absolute position of the reticle stage, wafer handling stage and projection lens system to improve pattern alignment.--

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PATENT NO. : 7,099,011

APPLICATION NO. : ~~10/727,081~~ 10/727,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 9, lines 56-57, please amend as follows:

--Then in block 3416 we reconstruct the overlay measurements that are used to produce the lens distortion map.--

Column 12, lines 16-28, please amend as follows:

--In another embodiment, if it is believed or there is evidence that the wafer stage and reticle alignment system are extremely accurate and repeatable (for example if the accuracy and repeatability <~ overlay metrology tool accuracy and repeatability), then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx4,Ty4,q4) can be set to zero in equations 5-8. Not solving for the T's and q's allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution that includes field rotation, orthogonality, and x and y scale is obtained if the constraints of equation 9 and equation 10 through equations 14 and 15 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=qo=sx=sy=0 in equations 20 and 21.

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CERTIFICATE OF CORRECTION

PATENT NO. : 7,099,011

APPLICATION NO. : ~~10/727,081~~ 10/724,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 16, lines 63-67, please amend as follows:

--With regard to error multipliers, the effect of including the R-shears in these calculations is to further reduce the error multipliers from the X, Y shear case since including more measurements increases the averaging of overlay metrology tool noise and thereby decreases ~~it's~~ its influence.--

Column 17, lines 7-20, please amend as follows:

--In another embodiment, if ~~its~~ it is believed, or there is evidence, that the wafer stage and reticle alignment system are extremely accurate and repeatable, for example if the accuracy and repeatability <~ overlay metrology tool accuracy / repeatability, then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx6,Ty6,q6) can be set to zero in equations 27-32. Not solving for the T's and q's allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution is obtained that includes field rotation and overall scale if the constraints of equation 33 and equation 34 through equations 37 and 38 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=s=0 in equations 41 and 42.--

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,099,011
APPLICATION NO.	:	~~10/727,081~~ 10/724,018
ISSUE DATE	:	August 29, 2006
INVENTOR(S)	:	McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 18, lines 28-53, please amend as follows:

--A variation of the first two embodiments that allows the user to extract the repeatable part of the intra-field distortion with a minimum number of exposed fields and overlay metrology is described. Below, Eo is the E-zero or minimum exposure dose required for a large, i.e. 200 micron at wafer, open area pattern on the reticle to become fully developed, or cleared in the case of positive resist. FIG. 34A illustrates a process flow diagram where in blocks 3442, 3444 and 3446, the overlay target reticle and resist coated wafer are loaded into the projection imaging tool, or machine, as described above. Next in blocks 3448 and 3450, instead of exposing each field with a single scanning or exposing action, the machine is programmed to expose each field at a multiplicity of lower doses. So if a*Eo (a > 1) is the required dose at the wafer to completely expose a single field with a single exposing action, we expose the field N times at a dose of a*Eo/N, where N is some predetermined number, typically 20. Within these N exposures the wafer stage is not moved to another field position, a single field is exposed N times. In the preferred embodiment, this process is repeated 3 more times for the other fields. The result of this procedure is to average out the scanning non-repeatability by an amount proportional to N (parameterized as b*M). The exact configuration of the resist (novolac, chemically amplified, resist manufacturer, processing conditions) determines whether b =1 or is < 1.--

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,099,011

APPLICATION NO. : ~~10/727,861~~ 10/724,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 18, lines 58-67, please amend as follows:

--Then in blocks 3452, 3454, and 3456 the wafer is developed and the overlay targets ~~and~~ are measured and a lens distortion map constructed as described above in connection with FIG. 34.

In another variation of the first two embodiments, multiple exposing actions are performed to average out the effect of non-repeatability, but now the overlay reticle, for example the reticle of FIG. 20, has a partially reflecting dielectric coating either on ~~it's~~ its non-chrome or possibly chrome coated (machine optical object plane) surface see FIG. 20C. For --

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PATENT NO. : 7,099,011

APPLICATION NO. : 10/727,081 10/727,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 19, lines 40-57, please amend as follows:

--The techniques described above have been mainly described with respect to alignment attributes that are in the form of a box in box or frame in frame pattern as shown in FIG. 14. Other alignment attributes such as gratings can be used. *See* U.S. Pat. No. 6,079,256 - Overlay Alignment Measurement of Wafer, *supra*, and FIG. 1b, wafer alignment marks. *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, *supra*, van der Pauw resistors. *See* Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography systems, *supra*, vernier pairs; *See* Method of Measuring Bias and Edge overlay error for sub 0.5 micron Ground Rules, C. Ausschnitt, et al., U.S. Pat. No. 5,757,507 (1998), capacitor structures. *See* Capacitor Circuit Structor For Determining Overlay Error, *supra* could be used instead. In general, any alignment attribute that can be used by an overlay metrology tool for measuring offsets can be utilized by the techniques described.--

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APPLICATION NO. : ~~10/727,081~~ 10/724,018

ISSUE DATE : August 29, 2006

INVENTOR(S) : McArthur et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE SPECIFICATION

Column 25, line 51 to column 26, line 20, please amend as follows:

--The techniques have been mainly described with respect to ~~it's~~ their application on the projection imaging tools such as photolithographic stepper ~~systems~~ systems. *See* Direct-referencing automatic two-points reticle-to-~~wafer~~ wafer alignment using a projection column servo system, *supra*; New 0.54 Aperture I-Line Wafer Stepper With Field by Field Leveling Combined with Global Alignment, M. Van den Brink, B. Katz, S. Wittekoek, SPIE Vol. 1463, 709:724, 1991; Projection optical system for use in precise copy, T. Sato, et al., U.S. Pat. No. 4,861,148, 1989, and photolithographic scanners systems. *See* Micrascan (TM) III performance of a third generation, catadioptric step and scan lithographic tool, D. Cote, et al., SPIE Vol. 3051, 806:816, 1997; ArF Step And Scan Exposure System For 0.15 Micron and 0.13 micron Technology Node, J. Mulkens, et al., SPIE Conference on Optical Microlithography XII, 506:521, March, 1999; 0.7 NA DUV step and Scan system for 150nm Imaging with Improved Overlay, supra ~~*supra*~~]) most commonly used in semiconductor manufacturing today. The techniques can be applied to other projection imaging tools such as contact or proximity printers. *See* Optical Lithography--Thirty years and three orders of magnitude, *supra*, 2-dimensional scanners; *See* Large-area, High-throughout, High-Resolution Projection Imaging System, K. Jain, U.S. Pat. No. 5,285,236, 1994, Optical Lithography--Thirty years and three orders of magnitude, *supra*, office copy machines, and next generation lithography (ngl) systems such as XUV. *See* Development of XUV projection lithography at 60-80 nm, *supra*, SCALPEL, EUV (Extreme Ultra Violet); *See* Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron ef 53, *supra*, IPL (Ion Projection Lithography), and EPL (electron projection lithography). *See* Mix-And-Match: A necessary Choice, *supra*. In addition, the techniques can be applied to a lithographic projection system used in an electron beam imaging system, or a direct write tool, or an x-ray imaging system.--

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Client #: 38203-6080C (DAH:msm)

Enclosures: Transmittal Letter, 1 page (in duplicate); Preliminary Amendment, 12 pages; This Postcard.

For: METHOD AND APPARATUS FOR SELF-REFERENCED PROJECTION LENS DISTORTION MAPPING

Applicant(s):. Smith et al.
Application No.: 10/727,081 – **Filed:** 12/02/2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Smith, *et al.*
Serial No.:	~~10/727,081~~ 10,727,018
Customer No.:	33123
Filed:	December 2, 2003
For:	*METHOD AND APPARATUS FOR SELF-REFERENCED PROJECTION LENS DISTORTION MAPPING*
Art Unit:	Unassigned
Examiner:	Unassigned

CERTIFICATE OF MAILING

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TRANSMITTAL LETTER

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Preliminary Amendment for filing in connection with the above-identified application. Because this Preliminary Amendment is filed prior to receipt of a first office action on the merits in the above-referenced application, no fee is due. However, should it be determined that a fee for filing these papers is required, the Commissioner is authorized to charge Deposit Account No. 50-1213, as stated below:

[X] The Commissioner is hereby authorized to charge any fees that may be due under 37 C.F.R. §§ 1.16-1.17 in connection with this paper or with this application during its entire pendency to Deposit Account No. 50-1213. A duplicate of this sheet is enclosed.

Respectfully submitted,
HELLER, EHRMAN, WHITE & McAULIFFE LLP

By: COPY
David A. Hall
Registration No. 32,233

Attorney Docket No.: 38203-6080C

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Email: dhall@hewm.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Smith, *et al.*
Serial No.:	~~10/727,081~~ 10/724,018
Customer No.:	33123
Filed:	December 2, 2003
For:	*METHOD AND APPARATUS FOR SELF-REFERENCED PROJECTION LENS DISTORTION MAPPING*
Art Unit:	Unassigned
Examiner:	Unassigned

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TRANSMITTAL LETTER

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Respectfully submitted,
HELLER, EHRMAN, WHITE & McAULIFFE LLP

By: _____
David A. Hall
Registration No. 32,233

Attorney Docket No.: 38203-6080C
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Smith, *et al.*
Serial No.:	~~10/727,881~~ 10/724,018
Customer No.:	33123
Filed:	December 2, 2003
For:	*METHOD AND APPARATUS FOR SELF-REFERENCED PROJECTION LENS DISTORTION MAPPING*
Art Unit:	Unassigned
Examiner:	Unassigned

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3/18/04 Anne Kopeck
Date Signature

PRELIMINARY AMENDMENT

Mail Stop Non-Fee Amendment
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Alexandria, VA 22313-1450

Sir:

In advance of the first examination in the above-identified patent application, Applicants request amendment in accordance with 37 C.F.R. § 1.121, as follows:

Amendments to the Specification begin on Page 2 of this paper.

Remarks begin on Page 10 of this paper.

Amendments to the Specification

Please amend the specification as follows:

Please amend the paragraphs beginning on page 5, line 16, through page 6, line 18, as follows:

Semiconductor manufacturing facilities generally use some version of the following complex overlay procedure to help determine the magnitude of lens distortion independent of other sources of systematic overlay error. The technique has been simplified for illustration. *See* Analysis of image field placement deviations of a 5x microlithographic reduction lens, D. MacMillen, et. Al., SPIE Vol. 334, 78:89, 1982. Figures 2 and 3 show typical sets of overlay targets 300, including – one large or outer box 302 and one small or inner target box 304. Figure 1 shows a typical portion of a distortion test reticle 102 used in the prior art. It should be noted that the chrome target patterns on most reticles are 4 or 5 times larger as compared with the patterns they produce at the image ~~plane,~~ plane; this simply means modern steppers are reduction systems. Further, for purposes of discussion, it is assumed that the reticle pattern is geometrically perfect, (in practice, the absolute positions of features on the reticle can be measured and the resulting errors subtracted off). First, a wafer covered with photoresist is loaded onto the wafer stage and globally aligned. Next, the full-field image of the reticle, 102 in Figure 1 is exposed onto the resist-coated wafer 2102 in Figure 21. For purposes of illustration, we assume that the distortion test reticle consists of a 5 x 5 array of outer boxes evenly spaced a distance M*P, across the reticle surface see Figure 1. It is typically assumed that the center of the optical system is virtually aberration free. *See* Analysis of image field placement deviations of a 5x microlithographic reduction lens, *supra*. With this assumption, the reticle, 102 in Figure 1 is now partially covered using the reticle blades, 1704 in Figure 17, in such a way that only a single target at the center of the reticle field, box 104, in Figure 1, is available for exposure. Next, the wafer stage is

moved in such a way as to align the center of the reticle pattern directly over the upper left hand corner of the printed 5 x 5 outer box array, wafer position ~~2100~~ 2106, Figure 21. The stepper then exposes the image of the small target box onto the resist-coated wafer. If the stepper stage and optical system were truly perfect then the image of the small target box would fit perfectly inside the image of the larger target box, as illustrated in Figures 4, and 21, from the previous exposure.

Please amend the paragraphs beginning on page 13, line 14, through page 16, line 8, as follows:

Overlay error is referred to as overlay registration ~~include,~~ including registration error and pattern placement ~~error,~~ error; for our work here, we will simply use the term overlay error or error. For classification purposes, overlay error is typically divided into the following two categories: grid or inter-field and intra-field error. Intra-field error is the overlay error in placement within a projection field, or simply field, of a lithographic projection system. Inter-field error is the overlay error from field to field on the wafer. The physical sources of these errors are generally distinct; inter-field error is due to imaging objective aberrations or possibly scanning dynamics while intra-field errors are due to the wafer alignment system and the wafer stage. The focus of this invention is determination of intra-field error.

In order to measure overlay error using conventional optical metrology tools, special alignment attributes or overlay target patterns, such as the ones shown in Figure 14, are printed or imaged onto a properly designed recording media using a photolithographic imaging system such as the one illustrated in Figure 17. Here recording media is meant to include: positive or negative photoresist, optically activated liquid crystals, CCD or diode imaging arrays, and photographic film. There are many different kinds of alignment attributes including, box-in-box 1402, frame-in-frame 1404 as shown in Figure 14, as well as gratings, verniers, and electrical test structures. *See* Automated Electrical Measurements of Registration Errors in Step

and Repeat Optical Lithography systems, T. Hasan, et. Al., IEEE Transactions on Electron Devices, Vol. ED-27, No. 12, 2304:2312, December, 1980; Capacitor Circuit Structure For Determining Overlay Error, K. Tzeng, et. Al., US Patent 6143621, 2000; Overlay Alignment Measurement of Wafers, N. Bareket, US Patent 607925, 2000. The present invention applies to photolithographic steppers, scanners, e-beam systems, EUV and x-ray imaging systems. *See* Mix-And-Match: A necessary Choice, *supra*; Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron, J. Bjorkholm, et. Al., Journal Vacuum Science and Technology,B 8(6), 1509:1513, Nov/Dec 1990; Development of XUV projection lithography at 60-80 nm, B. Newnam, et. Al., SPIE vol. 1671, 419:436, 1992; Optical Lithography – Thirty years and three orders of magnitude, J. Bruning, SPIE Vol. 3051, 14:27, 1997. Figure 28 shows a typical vector plot of overlay error measured with a commercial overlay tool using box-in-box structures. In some cases the overlay error can be measured using special in-situ exposure tool metrology. *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, M. Van den Brink, et. Al., SPIE VOL. 1087, 218:232, 1989. Vector displacement plots like these illustrated in Figure 28 give a visual description of the direction, magnitude, and location of overlay error, and are mathematically separated into components using variety of regression routines; Figures 28- 30 are a schematic of this while ~~See~~ Analysis of overlay distortion patterns, J. Armitage, J. Kirk, SPIE Vol. 921, 207:221, 1988 contains numerous examples. Many commercial software packages exist (Monolith, *See* A Computer Aided Engineering Workstation for registration control, *supra.*, Klass II; *See* Lens Matching and Distortion testing in a multi-~~stepper,~~ stepper, sub-micron environment, A.Yost, et. al., SPIE Vol. 1087, 233:244, 1989) that model and statistically determine the relative magnitude of the systematic and random inter-field and intra-field error components for the purpose of process control and exposure tool set-up. Once the inter-field and intra-field overlay data is analyzed the

results are used to adjust the calibration constants and absolute position of the reticle stage, wafer handling stage and projection lens system to improve pattern alignment.

Preferred Embodiment

A simple and accurate methodology that allows for the extraction of lens distortion placement error excluding total translation, rotation, orthogonality and x and y scale error and is mathematically decoupled from stage error is described. Figure 34 illustrates the methodology in terms of a process flow diagram. First, in block 3402, a wafer is provided; wafer alignment marks are not required, a bare wafer can be used. Next, in block ~~3402~~ 3404, the wafer is coated with resist and loaded onto the projection imaging system or machine. Then in block 3406, a reticle pattern such as illustrated in Figure 20, including a two dimensional array of box structures or targets of various sizes, see Figure 20A, is loaded into the machine's reticle management system and aligned to the reticle table. The reticle pattern be, for example, Nx x Ny array of overlay groups as shown in Figure 20A with a portion of the whole Nx x Ny array being schematically shown in figure 20.

Please amend the paragraph on page 17, lines 13-14, as follows:

Then in block 3416 we reconstruct the overlay measurements that are used to produce the lens distortion map.

Please amend the paragraph on page 21, lines 7-15, as follows:

In another embodiment, if it is believed or there is evidence that the wafer stage and reticle alignment system are extremely accurate and repeatable ~~for~~ (for example if the accuracy and repeatability <~ overlay metrology tool accuracy and repeatability), then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx4,Ty4,q4) can be set to zero in equations 5-8. Not solving for the T's and q's

allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution that includes field rotation, orthogonality, and x and y scale is obtained if the constraints of equation 9 and equation 10 through equations 14 and 15 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=qo=sx=sy=0 in equations 20 and 21.

Please amend the paragraph on page 29, lines 15-23, as follows:

In another embodiment, if ~~its~~ it is believed, or there is evidence, that the wafer stage and reticle alignment system are extremely accurate and repeatable, for example if the accuracy and repeatability <~ overlay metrology tool accuracy / repeatability, then all stage positioning and yaw errors (Tx1,Ty1,q1), . . . (Tx6,Ty6,q6) can be set to zero in equations 27-32. Not solving for the T's and q's allows determining the intra-field distortion uniquely to within an overall translation. That is, a unique solution is obtained that includes field rotation and overall scale if the constraints of equation 33 and equation 34 through equations 37 and 38 are imposed and then calculate (dxf, dyf) using the resulting Tx, Ty values and setting q=s=0 in equations 41 and 42.

Please amend the paragraph beginning on page 32, lines 5-21, as follows:

A variation of the first two embodiments that allows the user to extract the repeatable part of the intra-field distortion with a minimum number of exposed fields and overlay metrology is described. Below, Eo is the E-zero or minimum exposure dose required for a large, i.e. 200 micron at wafer, open area pattern on the reticle to become fully developed, or cleared in the case of positive resist. Figure 34A illustrates a process flow diagram where in blocks 3442, 3444 and 3446, the overlay target reticle and resist coated wafer are loaded into the projection imaging tool, or machine, as described above. Next in blocks 3448 and 3450, instead of exposing

each field with a single scanning or exposing action, the machine is programmed to expose each field at a multiplicity of lower doses. So if a*Eo (a > 1) is the required dose at the wafer to completely expose a single field with a single exposing action, we expose the field N times at a dose of a*Eo/N, where N is some predetermined number, typically 20. Within these N exposures the wafer stage is not moved to another field position, a single field is exposed N times. In the preferred embodiment, this process is repeated 3 more times for the other fields. The result of this procedure is to average out the scanning non-repeatability by an amount proportional to N (parameterized as b*M). The exact configuration of the resist (novolac, chemically amplified, resist manufacturer, processing conditions) determines whether b =1 or is < 1.

Please amend the paragraphs beginning on page 33, lines 1-21, as follows:

Then in blocks 3452, 3454, and 3456 the wafer is developed and the overlay targets ~~and~~ are measured and a lens distortion map constructed as described above in connection with Figure 34.

In another variation of the first two embodiments, multiple exposing actions are performed to average out the effect of non-repeatability, but now the overlay reticle, for example the reticle of Figure 20, has a partially reflecting dielectric coating either on ~~it's~~ its non-chrome or possibly chrome coated (machine optical object plane) surface see Figure 20C. For example, a 95% reflecting dielectric coating applied to the overlay reticle means that if there are 20 exposure sequences, at a dose of Eo each, the net effect is to expose the wafer with a dose of 2*Eo and to have effectively averaged over as many as 20 exposures. The advantage of this technique is that it is not limited by the machine's ability to do sub-Eo exposures. A further advantage of this technique is that since the exposure doses can be made at the same dose as used in production runs, the dynamics of

SEP 1 8 2006.

the scanner movement during the measurement sequence will be the same and therefore the intra-field error measured under identical operating conditions. Thus, if the production dose is a*Eo, the overlay reticle has a coating that reflects a fraction R of light incident on it, then the number of exposures (N) required to get a dose of b*Eo on the measurement wafer is:

$$N = 1 + \text{floor}(b/(a*(1-R)) \qquad \text{(eq 43)}$$

and

floor(x) = integer part of the real number x.

Please amend the paragraph on page 34, lines 9-20, as follows:

The techniques described above have been mainly described with respect to alignment attributes that are in the form of a box in box or frame in frame pattern as shown in Figure 14. Other alignment attributes such as gratings can be used. *See* U.S. Patent 6,079,256 - Overlay Alignment Measurement of Wafter, *supra*, and Figure 1b, wafer alignment marks *See* Matching Management of multiple wafer steppers using a stable standard and a matching simulator, *supra*, van der Pauw resistors. *See* Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography systems, *supra*, vernier pairs; *See* Method of Measuring Bias and Edge overlay error for sub 0.5 micron Ground Rules, C. Ausschnitt, et. Al., US Patent 5757507, 1998, capacitor structures. *See* Capacitor Circuit Structor For Determining Overlay Error, *supra* could be used instead. In general, any alignment attribute that can be used by an overlay metrology tool for measuring offsets can be utilized by the techniques described.

Please amend the paragraph beginning on page 45, line 5, through page 46, line 3, as follows:

The techniques have been mainly described with respect to ~~it's~~ their application on the projection imaging tools such as photolithographic stepper

systems. *See* Direct-referencing automatic two-points reticle-to-wafer alignment using a projection column servo system, *supra*; New 0.54 Aperture I-Line Wafer Stepper With Field by Field Leveling Combined with Global Alignment, M. Van den Brink, B. Katz, S. Wittekoek, SPIE Vol. 1463, 709:724, 1991; Projection optical system for use in precise copy, T. Sato, et. Al., US Patent 4861148, 1989, and photolithographic scanners systems. *See* Micrascan (TM) III performance of a third generation, catadioptric step and scan lithographic tool, D. Cote, et. Al., SPIE Vol. 3051, 806:816, 1997; ArF Step And Scan Exposure System For 0.15 Micron and 0.13 micron Technology Node, J. Mulkens, et. Al., SPIE Conference on Optical Microlithography XII, 506:521, March, 1999; 0.7 NA DUV step and Scan system for 150nm Imaging with Improved Overlay, ~~*supra*]]~~ *supra*, most commonly used in semiconductor manufacturing today. The techniques can be applied to other projection imaging tools such as contact or proximity printers. *See* Optical Lithography – Thirty years and three orders of magnitude, *supra*, 2-dimensional scanners; *See* Large-area, High-throughout, High-Resolution Projection Imaging System, K. Jain, US Patent 5285236, 1994, Optical Lithography – Thirty years and three orders of magnitude, *supra*, office copy machines, and next generation lithography (ngl) systems such as XUV. *See* Development of XUV projection lithography at 60-80 nm, *supra*, SCALPEL, EUV (Extreme Ultra Violet); *See* Reduction imaging at 14nm using multilayer-coated optics: Printing of features smaller than 0.1 micron ef 53, *supra*, IPL (Ion Projection Lithography), and EPL (electron projection lithography). *See* Mix-And-Match: A necessary Choice, *supra*. In addition, the techniques can be applied to a lithographic projection system used in an electron beam imaging system, or a direct write tool, or an x-ray imaging system.

REMARKS

Any fees that may be due in connection with this application throughout its pendency may be charged to Deposit Account No. 50-1213.

The Preliminary Amendment is provided to amend the specification to correct obvious typographical and grammatical errors. Changes are indicated by underlining to show additions and strikethrough to indicate deletions. A vertical bar is provided at the left margin to help locate the changes. No new matter has been added to the application.

In view of the amendments and above remarks, entry of the amendments and examination of the application on the merits are respectfully requested.

Respectfully submitted,
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